REMARKS

Claims 1-3, 5-13, and 15-21 are pending. The examiner's reconsideration of the objections and rejections in view of the amendments and remarks is respectfully requested.

The Specification has been objected to for an informality. The examiner stated essentially that the title of the invention is not descriptive. The title of the invention has been amended to "SYSTEM AND METHOD FOR EXECUTING A PROGRAM INCLUDING INSTRUCTIONS AND COMPILER DECODED INSTRUCTIONS." The examiner's reconsideration of the objection is respectfully requested.

The drawings have been objected to as failing to comply with 37 CFR 1.84(p)(5). The examiner stated that he was unable to find reference numbers 311-315 in the specification. The specification has been amended to correct the reference to the execution queues previously found in the paragraph beginning at page 12, line 3. The examiner's reconsideration of the objection is respectfully requested.

Claims 1, 7 and 13 have been objected to for informalities. In claim 1, the comma after the word "of" has been deleted. With respect to claim 7, the word "to" has been inserted after the phrase "decoded instruction". In claim 13, the word "decoded" has been amended to "predecoded". Reconsideration of the objections is respectfully requested.

Claims 1, 5-9, 11, 13 and 16-20 have been rejected under 35 U.S.C. 102(b) as being anticipated by Parady (USPN 5,933,627). The Examiner stated essentially that Parady teaches all the limitations of claims 1, 5-9, 11, 13 and 16-20.

Claim 1 claims, *inter alia*, "providing a program of instructions comprising a plurality of instructions of the first instruction form and a plurality of instructions of the second instruction

form, wherein the first instruction form are decoded by a decoder in an execution pipeline and the second instruction form are predecoded by a compiler." Claim 11 claims, *inter alia*, "a branch unit connected to an instruction fetch unit for the first instruction form and a sequencer for the second instruction form, wherein the sequencer controls a plurality of gates connected between a plurality of execution queues for storing decoded instructions of the first instruction form and the plurality of execution units."

Parady teaches a method and apparatus for switching between threads of a program (see Abstract). Parady does not teach "providing a program of instructions comprising a plurality of instructions of the first instruction form and a plurality of instructions of the second instruction form, wherein the first instruction form are decoded by a decoder in an execution pipeline and the second instruction form are predecoded by a compiler" as claimed in claim 1. Parady teaches an instruction cache and a decode unit through which all instructions are processed (see Figure 1 and col. 2, line 66-col. 3, line10). The instructions of Parady are not provided predecoded by a compiler, essentially as claimed in claim 1. The instructions of Parady are processed by the decoder, and for off-chip instructions, processed by a predecoder and the decoder. Thus, the instructions of Parady are not predecoded as claimed in claim 1. Parady fails to teach "providing a program of instructions comprising a plurality of instructions of the first instruction form and a plurality of instructions of the second instruction form, wherein the first instruction form are decoded by a decoder in an execution pipeline and the second instruction form are predecoded by a compiler" as claimed in claim 1.

Referring to claim 11, Parady teaches a plurality of instruction buffers storing different threads of a program (see Figure 3). Parady does not teach "a branch unit connected to an instruction fetch unit for the first instruction form and a sequencer for the second instruction

form, wherein the sequencer controls a plurality of gates connected between a plurality of execution queues for storing decoded instructions of the first instruction form and the plurality of execution units" (emphasis added). The instruction buffers of Parady are controlled by thread switching logic (see element 112 of Figures 3). The thread switching logic is a pointer-based system for selecting a next thread from the instruction buffers (see col. 3, lines 57-65). The thread switching logic is not a gate connected between an execution queue for storing decoded instructions of the first instruction form and an execution unit, essentially as claimed in claim 11. Therefore, Parady fails to teach all the limitations of claim 11.

Claims 5-9 depend from claim 1. Claims 13 and 16-20 depend from claim 11. The dependent claims are believed to be allowable for at least the reasons given for claims 1 and 11, respectively. At least claim 20 is believed to be allowable for additional reasons.

Claim 20 claims "wherein the second instruction form is a logical subset of the first instruction form, wherein the predecoded instructions of the second instruction form are statically stored in the plurality of buffers, and wherein the predecoded instructions of the second instruction form are control signals generated by a compiler and are not decoded during a runtime of the program."

Parady teaches a program of instructions that are decoded during a runtime. Parady does not teach a program of instructions and control signals, essentially as claimed in claim 20. Parady processes each instruction through the decoder or the decoder and the predecoder (see Figure 1). Therefore, Parady does not teach "wherein the predecoded instructions of the second instruction form are control signals generated by a compiler and are not decoded during a runtime of the program" as claimed in claims 20.

The examiner's reconsideration of the rejection is respectfully requested.

Claims 2 and 3 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Parady. The examiner stated essentially that the teachings Parady teach or suggest all the limitations of claims 2 and 3.

Claims 2 and 3 depend from claim 1. The dependent claims are believed to be allowable for at least the reasons given for claim 1. At least claim 2 is believed to be allowable for additional reasons.

Claim 2 claims "wherein the instructions of the first form and instructions of the second form are generated by a compiler, wherein instructions of the second form are statically loaded into the plurality of buffers as control signals ready for execution."

Parady teaches instructions decoded by a decode unit (see element 14 in Figure 1). Parady does not teach or suggest "wherein the instructions of the first form and instructions of the second form are generated by a compiler, wherein instructions of the second form are statically loaded into the plurality of buffers as control signals ready for execution." Parady teaches that instructions are processed by a decode unit. Parady does not teach or suggest a statically loaded control signal, essentially as claimed in claim 2. Therefore, Parady fails to teach all the limitations of claim 2.

Reconsideration of the rejection is respectfully requested.

Claims 10, 15 and 21 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Parady in view of Hennessy and Patterson "Computer Architecture – A Quantitative Approach, 2nd Edition" 1996. The examiner stated essentially that the combined teachings of Parady and Hennessy teach or suggest all the limitations of claims 10, 15 and 21.

Claim 10 depends from claim 1. Claim 15 depends from claim 11. The dependent claims are believed to be allowable for at least the reasons given for claims 1 and 11.

Claim 21 claims "the sequencer, engaged by the branch unit, adapted to fetch the predecoded instructions and sequence the predecoded instructions of the second instruction form, wherein the sequencer is connected to a plurality of gates connected between a plurality of execution queues adapted to store the decoded instructions of the first instruction form and the plurality of execution units, the sequencer further adapted to control the gates."

Parady teaches a plurality of instruction buffers storing different threads of a program (see Figure 3). Parady does not teach "a plurality of gates connected between a plurality of execution queues adapted to store the decoded instructions of the first instruction form and the plurality of execution units, the sequencer further adapted to control the gates" as claimed in claim 21. The instruction buffers of Parady are controlled by thread switching logic (see element 112 of Figures 3). The thread switching logic is a pointer-based system for selecting a next thread from the instruction buffers (see col. 3, lines 57-65). The thread switching logic is not a gate connected between an execution queue for storing decoded instructions of the first instruction form and an execution unit, essentially as claimed in claim 21. Therefore, Parady fails to teach all the limitations of claim 21.

Hennessy teaches reservation stations (see page 253, Figure 4.8). Hennessy does not teach or suggest "a plurality of gates connected between a plurality of execution queues adapted to store the decoded instructions of the first instruction form and the plurality of execution units, the sequencer further adapted to control the gates" as claimed in claim 21. The reservation stations of Hennessy are connected directly to the FP adders and FP multipliers. Hennessy does not teach or suggest a gate. Therefore, Hennessy fails to cure the deficiencies of Parady.

The combined teachings of Parady and Hennessy fail to teach or suggest "a plurality of gates connected between a plurality of execution queues adapted to store the decoded

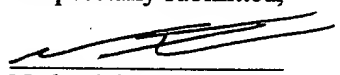
instructions of the first instruction form and the plurality of execution units, the sequencer further adapted to control the gates" as claimed in claim 21. The Examiner's reconsideration of the rejection is respectfully requested.

Claims 12 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Parady, in view of Ball and Larus, "Efficient Path Profiling," 1996. The examiner stated essentially that the combined teachings of Parady and Ball teach or suggest all the limitations of claim 12.

Claim 12 depends from claim 11. Claim 12 is believed to be allowable for at least the reasons given for claim 11. The examiner's reconsideration of the rejection is respectfully requested.

For the forgoing reasons, the application, including claims 1-3, 5-13, and 15-21, is believed to be in condition for allowance. Early and favorable reconsideration of the case is respectfully requested.

Respectfully submitted,



Nathaniel T. Wallace
Reg. No. 48,909
Attorney for Applicants

F. CHAU & ASSOCIATES, LLC
130 Woodbury Road
Woodbury, New York 11797
TEL: (516) 692-8888
FAX: (516) 692-8889